CBCS SCHEME

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15EC655

Sixth Semester B.E. Degree Examination, July/August 2021
Microelectronics

Time: 3 hrs. Max. Marks: 80

Note: Answer any FIVE full questions.

Important Note : 1. On completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages.
2. Any revealing of identification, appeal to evaluator and /or equations written eg, 42+8 = 50, will be treated as malpractice.

1 a. Derive an expression of drain current in NMOS transistor for triode and saturation regions, with necessary diagrams. **(08 Marks)**

b. Design the circuit shown in Fig.Q1(b) to obtain a current I_D of 80 μA. Find the value required for R and find the dc voltage V_D. Let the NMOS transistor have V_t = 0.6 V, $\mu_n C_{ox}$ = 200 μA/V^2, L = 0.8 μm and w = 4 μm. Neglect the channel-length modulation effect (i.e. assume λ = 0).

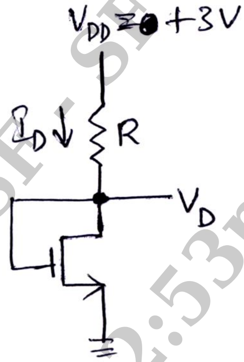

Fig.Q1(b) **(04 Marks)**

c. Explain the effect of substrate bias on threshold voltage of MOS transistors. **(04 Marks)**

2 a. With a neat diagram, explain the operation of enhancement-type NMOS transistor in detail. **(08 Marks)**

b. An NMOS transistor is fabricated in a 0.4 μm process having $\mu_n C_{ox}$ = 200 μA/V^2 and V'_A = 50 V/μm of channel length. If L = 0.8 μm and W = 16 μm, find V_A and λ. Find the value of I_D that results when the device is operated with an overdrive voltage V_{OV} = 0.5 V and V_{DS} = 1V. Also find the value of r_0 at this operating point. If V_{DS} is increased by 2V, what is the corresponding change in I_D? **(08 Marks)**

3 a. With a neat diagram, explain the operation of the common-source amplifier. Also derive the expressions for input and output resistance and voltage gain. **(10 Marks)**

b. Explain briefly the MOSFET internal capacitances. **(06 Marks)**

4 a. Explain the biasing of MOSFET using constant current source. **(06 Marks)**

b. Explain the small signal model of MOSFET and how the T-equivalent circuit model can be obtained. **(06 Marks)**

c. A MOSFET is to operate at I_D = 0.1 mA and is to have g_m = 1 mA/V. If K'_n = 50 μA/V^2, find the required (W/L) ratio and the overdrive voltage. **(04 Marks)**

5 a. Compare the following characteristics of MOSFET and BJT:
(i) Transconductance g_m
(ii) Intrinsic gain A_o **(04 Marks)**

b. Given V_{DD} = 3V and using I_{Ref} = 100 μA, it is required to design the circuit of Fig.Q5(b) to obtain an output current whose nominal value is 100 μA. Find R if Q_1 and Q_2 are matched and have channel lengths of 1 μm, channel widths of 10 μm, V_t = 0.7 V, and K'_n=200 μA/V^2. What is the lowest possible value of V_0? Assuming that for this process technology the early voltage V'_A = 20 V/μm, find the output resistance of the current source. Also, find the change in output current resulting from a +1V change in V_0.

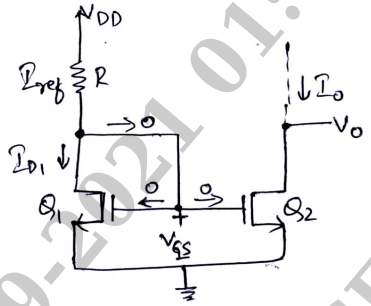

Fig.Q5(b) **(06 Marks)**

c. Derive the expression for determining the 3-dB frequency (ω_H) of an amplifier. **(06 Marks)**

6 a. Explain briefly the operation of MOS current steering circuit. **(06 Marks)**

b. For the circuit shown in Fig.Q6(b), find the midband voltage gain $A_m = V_0/V_{sig}$ and the upper 3-dB frequency f_H. Where R_{sig} = 100 KΩ, R_{in} = 420 KΩ, $C_{gs} = C_{gd}$ = 1 PF, g_m = 4 mA/V and R'_L = 3.33 KΩ.

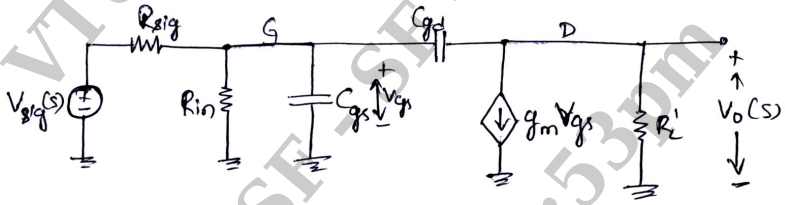

Fig.Q6(b) **(06 Marks)**

c. The high frequency response of an amplifier is characterized by the transfer function.

$$F_H(s) = \frac{1-\frac{s}{10^5}}{\left(1+\frac{s}{10^4}\right)\left(1+\frac{s}{4}*10^4\right)}$$

Determine the 3-dB frequency approximately and exactly. **(04 Marks)**

7 a. Explain the high frequency response of the CS amplifier and analyze using Miller's theorem. **(08 Marks)**

b. Consider a common-gate amplifier specified as follows:
W/L = 7.2 μm/0.36 μm, K'_n = 387 μA/V^2, r_0 = 18 KΩ, I_D = 100 μA, g_m = 1.25 mA/V, x = 0.2, R_S = 10 KΩ, R_L = 100 KΩ, C_{gs} = 20f F, C_{gd} = 5f F and C_L = 0. Find A_{V_o}, R_{in}, R_{out}, G_v, G_{is}, G_i and f_H. **(08 Marks)**

8 a. Explain the operation of MOS cascode amplifier. **(08 Marks)**

b. Explain the effect of source resistance on transconductance and voltage gain of a CS amplifier. **(08 Marks)**

9 a. Explain the operation of MOS differential pair with a common mode input voltage. **(08 Marks)**

b. Explain the effect of g_m mismatch on CMRR of a MOS differential amplifier. **(08 Marks)**

10 a. With a neat diagram, explain the operation of a two-stage CMOS op-amp. **(08 Marks)**

b. Obtain the expression for differential gain of the active-loaded MOS pair. **(08 Marks)**

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